F28P55x编程实例Labs_CLB

- Code Composer Studio
- > C2000Ware
- LaunchXL-F28P55x



Configurable Logic Block, 可配置逻辑块

- ▶ 一组模块的集合
- ▶ 模块通过软件进行互联
- ▶ 自定义数字逻辑功能
- ▶ 增强片上外设







功能实现

EPWM系统正常运行时,GPIOO输出方波。用GPIO来模拟一个 传感器,

- 当传感器输出低电平时, EPWM系统正常运行, 输出方波;
- 当传感器输出高电平时, EPWM系统停止运行, 输出低电平;

实现步骤

- ▶ 复制空白工程
- ➢ Sysconfig配置GPIO
- ➢ Sysconfig配置EPWM
- ➢ Sysconfig配置CLB
- ▶ 编写应用代码
- ▶ 模拟传感器故障,查看系统运行状态





GPIO	用途
myGPIOSensor	模拟传感器输入
LED_EPWM_GPIO	指示正常运行模式
LED_SENSOR_GPIO	指示故障运行模式

ab_clb_launchpad.syscfg × 🙆 lab_r	nain.c		-
👻 Type Filter Text	× ← → Software + GPI0		👝 🛛 🗉 😐 🗄
C SYSTEM (18)	⊕ GPIO (3 of 66 Added) ⊚		ADD FREMOVE ALL
	myGPIOSensor		0 0
CLB OUTPUTXBAR	OmyBoardLED0_GPI0		6 5
CLEXBAR 7/11 😋 (CPUTIMER (OmyBoardLED1_GPI0		0 8
DCC	D Name	myGPIOSensor	
EPWMXBAR (Duse Hardware	None	
ELASH	Analog Mode	Þís is in digital mode.	
GPIO 1/66 🥝 (GPIO Direction	Pin is a GPI0 input	*
INPUTXBAR IN_ 1/16 🥝 (Pin Type	Push-pull output/floating input	
INTERRUPT 1 S	Qualification Mode	Synchronization to SYSCLK	*
OTHER	External Interrupts Connect to an XINT for interrupts		×
SYSCTL (⊕ ⊋) Core Select	CPU1 selected as controller core	÷
WATCHDOG	Write Initial Value		
 ANALOG (6) ADC 	PinMux Peripheral and Pin Configuration		×
ANALOG PinMux (ASYSCTL (CMPSS (● GPI0 ● ● 	GPI027/59 (SPIB BP)	- 8
DAC	(C)		

配置GPIO

配置GPIO

GPIO	用途
myGPIOSensor	模拟传感器输入
LED_EPWM_GPIO	指示正常运行模式
LED_SENSOR_GPIO	指示故障运行模式

§ lab_clb_launchpad.syscfg × iii lab_ma	in.c		e 0
😰 😤 Type Filter Text	\times \leftarrow \rightarrow Software = INPUTXBAR INPUT		() <> E () :
AID (18)	INPUTXBAR INPUT (1 of 16 Added)		⊕ ADD ■= REMOVE ALL
CLA ①	@myINPUTXBAR1		6 8
E CLB OUTPUTXBAR 💮	Name	myINPUTXBAR1	
CLBXBAR 1/II 🔮 🕀	INPUT	XBAR_INPUT1	*
CPUTIMER (INPUT Source	GPI027	÷
EDWMXBAR	Selected Source Of GPI0	myGPI05enpor = 6PI027	
ERAD (+)	INPUT Lock		
FLASH 🛞			
GPIQ 3/66 😋 🕀			
INPUTXBAR IN., 1718 🥑 🕀			
INTERRUPT 1 💕 🕁			



配置GPIO

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LED_EPWM_GPIO	指示正常运行模式
LED_SENSOR_GPIO	指示故障运行模式

8 lab_clb_launchpad.syscfg	× Ic lab_main.	¢.		7.0
📰 \Xi Type Filter Sext.	×	← → Software + CLBXBAR		
SYSTEM (18)	Ð	CLBXBAR (1 of 8 Added)		⊕ ADD
	1/16 😋 🕀	@myCLBXBAR0		6 6
CLB OUTPUTXBAS	₹ ⊕	Name	myCLBXBAR0	
CLEXBAR	110 🚫 🕀	Aux Signal Input	AUX560	•
GPOTIMEN	0	Invert Mode		
EPWMXBAR	•	Auto Enable Mux Setting From Source		
ERAD FLASH	⊕ ⊕	Mux Selection Method		A
GPIO	1/00 🔮 🕀	MUXes to be used	MUX 01	
INPUTXBAR IN INTERRUPT	1 0 0	MUX 1 Config	CLB MUX01 INPUTXBAR1 INPUT	*



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LED_SENSOR_GPIO	指示故障运行模式

<pre>\$ lab_clb_launchpad.syscfg × in lab</pre>	main.c			- (
😨 🐨 Type Filter Test	×	← → Hardware + LED4		
GG GG G	₽+	LED4 () SmyBoardLED0_GPI0		OREMOVE BORTWARE
SW2	₽+	SmyBoardLED0		-
SCIA BP	+	Name	myBoardLEDQ_GPi0	
I2CB BP	+	Use Hardware	LED4	+
EPWM1 BP	+	Analog Mode	Pin is in digital mode	19
EPWM2 BP	+	GPIG Direction	Pin is a GPI0 output	
EPWM6 BP	+	Pin Type	Push-pull output/floating input	•
LINA BP	+	Qualification Mode	Synchronization to SYSCLK	1341
MCANA BP	+			
 Site 2 Standard BP 	÷	External interrupts Connect to an XINT for interrupts		*
SDIB BD	1	Core Select	CPU1 selected as controller core	
I2CA BP	+	Write Initial Value	2	
EPWM7 BP	+	Initial Value	0: GPIO state is LOW	-
EPWM4 BP	+			
EPWM5 BP	+	PinMux Peripheral and Pin Configuration		~
MCANB BP	+			
CAN Route Switch	_			
EQEP1 Header	Ð			
EQEP3 Header	•			
1604	00			
LEDS				





GPIO	用途
myGPIOSensor	模拟传感器输入
LED_EPWM_GPIO	指示正常运行模式
LED_SENSOR_GPIO	指示故障运行模式

E	😴 Type Filter Text	×	-
.r¢	✓ LAUNCHPAD F28P55X (12)	LEDS
HC.	 Boot Switches 		
圓	SW1		0
-	SW2	≡+	
王	 Site 1 Standard BP 		
	SCIA BP	+	Na
	SPIA BP	+	10
	(2C8 BP	+	
	EPWM1 BP	+	AR
	EPWM2 BP	+	GP
	EPWM6 BP	+	Pir
	LINA BP	+	00
	MCANA BP	+	14.9
	 Site 2 Standard BP 		E)
	SCIB BP	+	
	SPIB BP	+	Co
	12CA BP	+	W
	EPWM7 8P	+	Init
	EPWM4 8P	+	
	EPWM5 BP	+	P
	MCANB BP	+	
	CAN Route Switch		
	EQEP1 Header	()	
	EQEP3 Header	()	
	FSI Header	174	
	LED4	00	
	LED5	0	1

Blab_clb_launchpad.syscfg × 🗟 tab_t	main.c			
😰 😤 Type Filter Text	×	← → Hardware + LED5		👝 🛛 🖩 🔴 🗄
C LAUNCHPAD F28P55X (12)		LED5 (t)		HEMOVE BOFTWARE
SW1 SW2 Site 1 Standard BP	≡+ ≡+	@myBoardLED1_GPI0 @myBoardLED1		-
SCIA BP	+	Name	nyBoardLED1_GPI0	
12C8 8P	+	Use Hardware	1700 K (1910 K)	
EPWM1 BP	+	Analog Mode	Pin is in digital mode	. ×.
EPWM2 BP	+	GPIO Direction	Pin is a GPIO output	
EPWM6 BP	+	Pin Type	Push-pull output/floating input	
LINA BP MCANA BP	++++	Qualification Mode	Synchronization to SYSCLK	7
✓ Site 2 Standard BP		External Interrupts Connect to an XINT for interrupts		~
SCIB BP SPIB RP	+++++	Core Select	CPU1 selected as controller core	*
12CA BP	+	Write Initial Value		
EPWM7 BP	+	Initial Value	1: GPIO state is HIGH	
EPWM4 8P	+			
EPWM5 BP	+	PinMux Peripheral and Pin Configuration		~
MCANB 8P	+			





Time Base Period
$$= \frac{f_{tbclk}}{2f_{pum}} = \frac{100*10^6}{2*2000} = 25000.$$

lab_clb_launchpad.syscfg =lab_m	iain,c		-
😨 😤 Type Filter Text	× ← → Software → EPWM	0	
SYSTEM (18) AIO	© myEPWM0		60
	Name	myEPWM0	
	D Use Hardware	None	
CLBXBAR 1/8 OG CPUTIMER	Load EPWM Settings From Device Memory Export		~
EPWMXBAR G	0 D Copy Settings		*
FLASH GRID GPIO D/116 🥥 🖯	Template Code Generation		*
INPUTXBAR IN 1/10 @ @ INTERRUPT 1 @ @	EPWM Global Load		×.
OTHER	EPWM Time Base		
OUTPUTXBAR	Erredation Mode	Stop after next Time Base counter increment or decrement	
SYSCTL G	Ð	Divide clock by 1	-
WATCHDOG (6)	D Time Base Clock Divider	For perfectly synchronized TBCLKs across multiple EPWM modules, th the TBCTL register of each EPWM module must be set identically	e prescaler bits in
ADC G	High Speed Clock Divider	Divide clock by 1	1. K.
ANALOG PITIMUX G	Time Base Period Load Mode	PWM Period register access is through shadow register	
CMPSS	Time Base Period Load Event	Shadow to active load occurs when time base counter reaches 0	
DAC	D Time Base Period	25000	
PGA G	D Time Base Beried Link	Disable Linking	2. Q
 CONTROL (5) 	Enable Time Base Berind Global Load		
CLB 1/2 🕑 🤆	Initial Counter Value		
EDWIN 1072 CO	Counter Value	Un - Anne - court mode	
	Counter Made	Device down a file over allest	12
SYNC 1/1 O	D South One of Black	Count over anter sync even	
- COMMUNICATION (10)	Enable Prisse Shift Load		
DMA	B Force a Sync Pulse		
FSIRX	Sync in Pulse Source	Sync-in source is EPWM1 sync-out signal	- T.
FSITX	Sync Out Pulse	Boftware force generated EPWM sync-out pulse	
120	Dine-Shot Sync Out Trigger	Trigger is OSHT sync	•
MCAN G	EPWMxSYNCPER Source Select	Counter equals Period	



	EPWM Counter Compare	^
	CMPA	^
	Counter Compare A (CMPA)	12500 A rt is recommended to use a non-zero counter compare value when using shadow to active load of action qualifier A/B control register on TBCTR=0 boundary(<u>Un-suppress</u>)
Counter Compare Value = $(1 - \frac{duty}{100}) * tbprd = (1 - \frac{50}{100}) * 25000 = 12500$	Enable Counter Compare A (CMPA) Global Load	
	Enable Shadow Counter Compare A (CMPA)	
	Counter Compare A Shadow Load Event	Load when counter equals zero 👻
	Counter Compare A (CMPA) Link	Disable Linking 👻



EPWM Action Qualifier		
Enable Continuous SW Force Global Load		
Continuous SW Force Shadow Mode	Shadow mode load when counter equals zero	
	Digital compare event A 1	
T1 Trigger Source	T1/T2 selection and configuration of a trip/digital-com configuration of that event in the Trip-Zone submodule	npare event is indpendent of the
	Digital compare event A 1	
T2 Trigger Source	T1/T2 selection and configuration of a trip/digital-con configuration of that event in the Trip-Zone submodule	npare event is indpendent of the
ePWMxA Output Configuration		^
ePWMxA Global Load Enable		
ePWMxA Shadow Mode Enable		
ePWMxA Shadow Load Event	Load when counter equals zero	*
ePWMxA One-Time SW Force Action	No change in the output pins	*
ePWMxA Continuous SW Force Action	Software forcing disabled	*
ePWMxA Event Output Configuration		^
ePWMxA Time base counter equals zero	No change in the output pins	*
ePWMxA Time base counter equals period	No change in the output pins	*
ePWMxA Time base counter up equals COMPA	Set output pins to High	*
ePWMxA Time base counter down equals COMPA	Set output pins to low	•
ePWMxA Time base counter up equals COMPB	No change in the output pins	*
ePWMxA Time base counter down equals COMPB	No change in the output pins	*
ePWMxA T1 event on count up	No change in the output pins	*
ePWMxA T1 event on count down	No change in the output pins	*
ePWMxA T2 event on count up	No change in the output pins	*
ePWMxA T2 event on count down	No change in the output pins	



PinMux Peripheral and Pin Configuration		
EPWM Peripheral	EPWM1	<u>▼</u>
EPWM_A	GPIO0/79 (EPWM1 BP) Connected to hardware(<u>Un-suppress)</u>	▼ [
EPWM_B	GPI01/78 (EPWM1 BP) Connected to hardware(<u>Un-suppress)</u>	



配置CLB

 Alteriation (Lewister) 	X ← → Software → CLB		00000
FLASH	CLB (1 of 2 Added) ①		ADD ■ REMOVE A
INPUTXBAR IN. 1/16 CO G			5.0
INTERRUPT 1 🔮 🤅	Ø myCL81		
MEMCFG	Name	myCLB1	_
OTHER	CLB Instance	CLB1	3
OUTPUTXBAR (9	Enable CLB		
WATCHDOC G		Output 0	
ANALOG (A)	9 Overriding Outputs	CLB Output 0 is overriding the EPWM1A signal.	-
ADC G	Lock Overriding Outputs Setting		
ANALOG PinMux	HLC Generates NMI		
ASYSCTL G	5	-	
CMPSS	Clock Prescalar CLB input prescalar configuration		~
DAC			
PGA	Data Exporting Through SPI Buffer		~
CONTROL (5)	Inputs Used	Input 0, Input 1	
CLB HE CO			_
EPWM 1/12 🚱 🤆	CLB Input 0 CLB Input Configuration Input 0		
EQEP	Input Type Input 0	Use Global Mux	
SYNC 1/1 3	Global Mux Input 0	EPWM1A (CLB 1-4)	
COMMUNICATION (10)	Enghia Sung Ionut 0		
DMA G) enable Shici input o		
FSIRX	Input Filter Input 0	No Hitering	
FSITX	Input Pipeline Input 0		
120			
LIN	CLB Input 1 CLB Input Configuration Input 1		^
MCAN (4	Input Type Input 1	Use Global Mux	
PMBUS (Clobal Musterut 1	CLE V.BAP 4UVSICO	
SPI G			
USB G	2 Enable sync input 1		
SOFTWARE (2)	Input Filter Input 1	No filtering	
Device Support	Input Pipeline Input 1		
Software Prioritized Inter	Depister Internut Handler		
BOARD COMPONENTS (3)	Attack a TUE Coolis to this CID		
FSI	Attach a FILE Config to this CLB		
150 1 0 0	Initialize TILE		



配置CLB

CLB Interrupt	^
Name	myCLB1_INT
Interrupt Name	INT_myCLB1
Interrupt Handler	INT_myCLB1_ISR
Enable Interrupt in PIE	



配置CLB-LUT(Look-Up Table)

ab_clb_launchpad.syscfg × 🗟 lab_ma	in.c	= <u>0</u>
➡ Type Filter Text	\times \leftarrow \rightarrow Software $*$ Tile Design	
e PMBUS ⊕ & SCI ⊕	Global Parameters Settings that affect all instances	Ý
] SPI ① USB ①	Tile Design (1 Added) 🗇	● ADD III REMOVE ALL
E ~ SOFTWARE (2) Device Support	O TILE1	D D
Software Prioritized Inter (+)	Name	TILE1 To utilize the CLB simulation, please see the "Generate CLB Simulation File" description within the Global Parameters in the Tile Design module.
LED 2 🥝 🕘	Pipeline Mode	
SWITCH CONFIGURABLE LOGIC BL.	LL Configuration Options	~≪ []
Tile Design 1 🔮 🕀	Bundary Inputs (Simulation Only) TILE1	T1 = PWM, When i1== 0;
DCSM UINKER COMMAND FILE C	Look-Up Table 0 TILE1	T1 = 0, When i1 == 1;
 C2000WARE LIBRARIES (6) FATFS (1) 	Look-Up Table 1 TILE1	
✓ CALIBRATION (1)		
HRPWM SFO	Inout 0	Boundary input 0
V CONTROL (4)	Input 1	Boundary input 1
CONTROLLER (+)	Input 2 Sensor	Zero
REFGEN (4)	Input 3	Zero
TCM ①		
✓ MATH (2) FPUfastRTS ⊕	Look-Up Table 2 TILE1	: A
IQmath 🕒	LUT User Description	
✓ DSP (4)	Logic Equation	10
FFT ()	Input 0	Boundary input 1
Vector (+)	Input 1	Zero *
VCRC (4)	Input 2	Zero 👻
V COMMUNICATIONS (1)	Input 3	Zero



配置CLB-OUTLUT0(Output Look-Up Table 0)

Output Look-Up Table 0	TILE1
User Description	
Output Logic Equation	
Input 0	
Input 1	
Input 2	



配置CLB-HLC (High Level Controller)			
High Level Controller TILE1		<u>^</u>	
User Description			
Event 0 (e0)	Boundary input 1		
Event 1 (e1)	LUT 2 Output		
Event 2 (e2)	Zero		
Event 3 (e3)	Zero	v	
Register 0-3 Initialization		~	
FIFO Initialization and Refill Values		~	
Data Exporting Through SPI Buffer (Simulation Only)		~	
Other Dependencies		^	
HLC Program 0			
Instruction 0	INTR 1		
Instruction 1			
HLC Program 1		^	
Instruction D	INTR 2		
Instruction 1			
HLC Program 2		~	
HLC Program 3		~	



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